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				APPLICANT Junko IWANAGA, et al.			
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U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
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/JL/		EP 0 623 963	11-9-1994	SIEMENS AG			
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
/JL/		KEDZIERSKI et al., "High-Performance Symmetric-Gate and CMOS-Compatible Vt Asymmetric-Gate FinFET Devices", International Electron Devices Meeting 2001, IEDM Technical Digest, Washington DC, Dec. 2-5, 2001, New York, NY: IEEE, pp1951-1954, XP010575161					
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/John Lin/				06/20/2007			

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